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Design of a novel testable reversible Alu in QCA technology for high-performance nanocomputing

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Abstract
Quantum-dot Cellular Automata (QCA) has become one of the worthy studies for Nano-scale computing because we can achieve to low power consumption and high operating frequency by the design of reversible structures based on QCA technology. For this reason, this paper presents a novel fault-tolerance reversible ALU (Arithmetic Logic Unit) in QCA. Firstly, we have designed a new 3×3 RUG (Reversible Universal Gate), this gate achieves the lowest cost and overall cost between the best previous designs a reduction of 48.60% and 54.74%, respectively. Also, the proposed reversible ALU has analyzed with two main part RLU (Reversible Logic Unit) and RAU (Reversible Arithmetic Unit), the simulation results demonstrate that the proposed QCA designs are optimal in terms of circuit complexity and number of MVs (Majority Voters) in comparison with the other architectures, in our design coplanar crossover design approach is used. All proposed architectures are simulated using QCA Designer tool version 2.0.3.

Keywords: QCA cell, reversible gate, reversible arithmetic unit, reversible logic unit, QCA designer tool.

1. Introduction

In the past decades, CMOS technology has been used to design computer circuits and digital systems. But according to Moore's law, the number of devices integrated on chips will double in every 18 months [1], this means that CMOS technology has faced physical limits. Hence, challenges such as high power consumption, leakage current and fabrication cost forced the researchers to find a replacement for this technology [2]. So far, many researchers are investigating the new design methods such as Quantum-dot Cellular Automata (QCA) and reversible computing in order to overcome the current major challenges. Craig Lent offered initially the concept of QCA technology in 1993, it is a suitable replacement for CMOS technology in Nano-scale level due to low power consumption and high speed devices [3]. The basic component of QCA can be seen as a square quantum cell in which four quantum dots are positioned in each corner of a cell, this cell includes two free electrons that can move [4]. The reversible logic circuits are one of the best choices for overcoming the energy dissipation, power consumption and complexity design in logic circuits, in these circuits should be existed a one to one relationship between the input vector and output vector and the number of outputs are equal to the number of inputs. In 1967, Landaure's research showed that heat dissipation for losing any bit of information in irreversible logic is kTln2 Joules, where k is Boltzmann's constant (1.38×10-23 J/K) and T is the absolute temperature of operation [5]. Bennett in 1973 demonstrated that if a circuit only consists of reversible gates, this amount of energy will not dissipate [6]. One of the main basic of computational units is the Arithmetic Logic Unit (ALU) [7], this paper depicts the novel one-bit ALU in QCA technology which performs better than the other logical designs. ALU can implement arithmetic operation like to add, subtract, comparison and logical operation such as AND, OR and XOR. ALU is an important element of any processor. Therefore, design an ALU with low power consumption, and high speed is an important issue. In this paper a new 3×3 reversible gate is proposed which can implement in QCA technology. This gate has lower cell count, delay, cost and overall cost in comparison to the other existing works. Then, a novel efficient reversible ALU consisting of RAU (Reversible Arithmetic Unit) and RLU (Reversible Logic Unit) is designed by using the proposed reversible gate. The main goal of all designs is reduced cell count (complexity), delay, size and power consumption, in addition computing speed. Also, these structures use fewer garbage outputs and a constant number of inputs. Finally, all proposed structures are simulated using QCA Designer simulation tool.

The rest of this paper is organized as follows

In section 2, we introduce the basic concepts of this study. We provide a review on the previous works in section 3. In section 4, a new reversible gate is considered and the main functions are implemented with this reversible gate, then various analyzes are performed of this gate. In section 5, we present a new reversible ALU that includes RLU and ALU reversible circuits, as well as simulation results, and compared with the other available designs are offered in this section. Finally, this paper will be concluded in section 6.

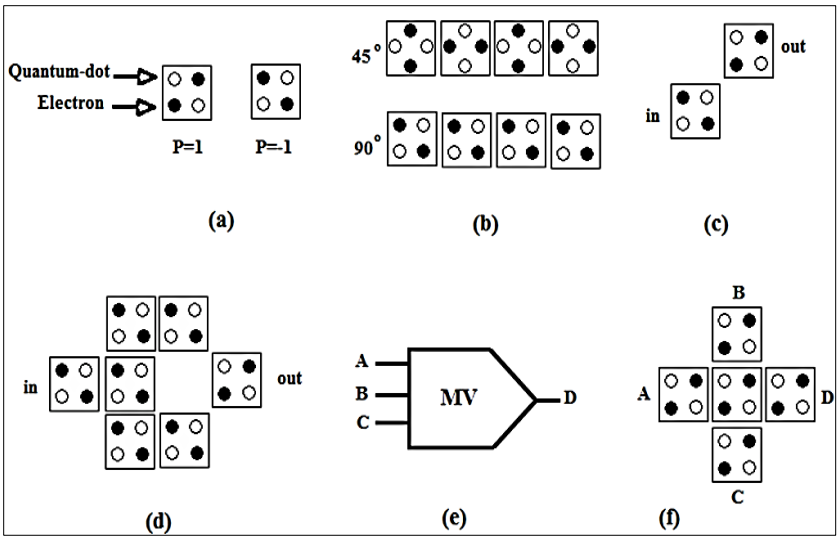
2. Fundamental of research

In this section, we discuss some basic concepts of reversible logic and QCA technology such as logic structure, wire-crossing, basic gates and clocking.

2.1 QCA background

The basic element of QCA is a QCA cell which is shown in Fig.1 (a). QCA cell has four quantum-dots which are placed at the corner of a square. In a QCA cell there are two additional mobile

electrons that are able to tunnel between quantum-dots. But tunneling outside of a cell is impossible. The position of these electrons creates two types of polarizations i.e. P = +1 to represent logic '1'and P =-1 to represent logic '0'. A wire can be built by placing several QCA cells in a row. There are two kinds of wires i.e. Ordinary wire (90º) and rotated wire (45º), which are shown in Fig.1 (b). The majority and inverter gates act as the basic gates in QCA. The two types of inverter are presented in Fig.1 (c) and Fig.1 (d). As are illustrated in Fig.1 (e) and Fig.1 (f), the majority gate has three inputs and five cells (three inputs, a middle cell, and one output). If assumed A, B and C are inputs to the majority gate, then the output is given by: M (A, B, C) = A.B+A.C+B.C, according to the logical function of the majority gate, Two-input OR and two-input AND gates can be realized using three-input Majority Voters (MVs) if the constant value of 1 or 0 is assigned to one of the input cells (Eq. (1) and Eq. (2)) [8].



$$M(A, B, 0) = A.B \quad (1)$$

$$M(A, B, 1) = A + B \quad (2)$$

Fig 1: Basic QCA structures. (a) QCA cell, (b) binary wire (90º) and inverter chain (45º), (c, d) inverter gate, (e) a Schematic view and (f) b QCA design of Three-input majority gate.

2.2 QCA clocking

On QCA technology, clocking controls the current data and it is required to synchronize and provide the necessary power for simulating a QCA circuit [9]. QCA has four clock zones, namely clock zones 0, 1, 2 and 3. Each clock zone consists of four phases i.e. Switch, hold, release and relax, as shown in Fig.2. During the switch phase, the inter-dot barriers are slowly raised and push the electrons into the corner dots. In this phase, electrons in the cell are placed according to the status of the input cell. In the hold phase, the inter-dot barriers are kept high and the locations of electrons remain constant and the cell can be used as an input for the cells of the next clock zone. During the release phase, the barriers are reduced. In the relax phase, the barriers are kept low and the cells have no polarization.

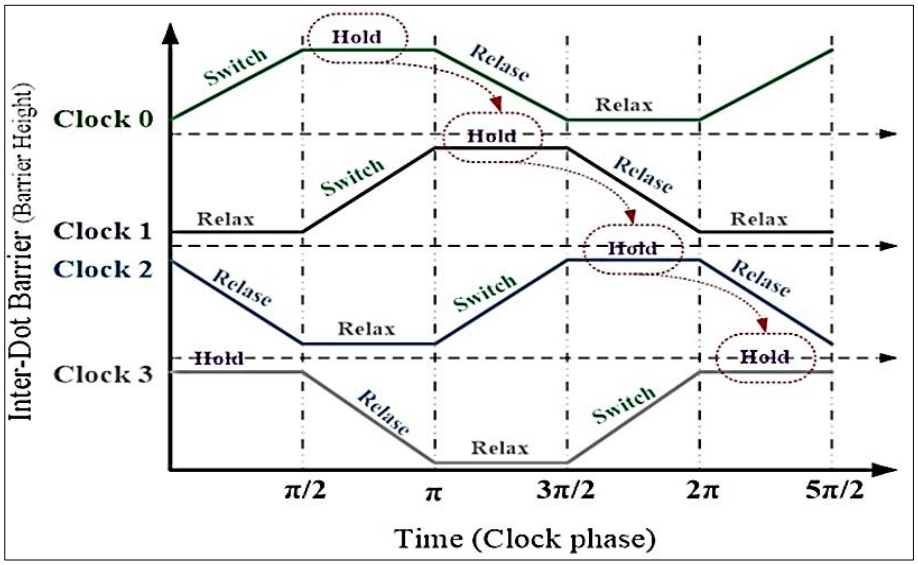


Fig 2: QCA clocking with four phases.

2.3 Reversible logic

A reversible logic gate is an N input and N output, in these circuits, the inputs can be recovered from the outputs, and the outputs can be determined from the inputs [10, 11]. A reversible circuit is made of reversible logic gates and it should be designed with the minimum number of reversible gates. In reversible circuit the garbage outputs are the outputs that would not be used in other computations and the constant inputs are the inputs whose values do not change in and have to be kept at 0 or 1 in order to implement the intended function, these inputs are also added to a structure for can make it reversible [11]. In reversible circuit fan-out and feedback is not allowed. The complexity of reversible circuits depends on some parameters like: number of reversible gates, number of constant inputs, number of garbage outputs and quantum cost, the quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates. Several of the important logic gates are Feynman Gate, Fredkin Gate, Toffoli Gate and Peres Gate.

3. Related works

Thus far, various Designs of reversible gates have been introduced which can be executed in QCA technology. Authors in [12] proposed a new optimized structure for different reversible gates (the gates like Feynman, Toffoli and Fredkin) by using a compact 2-input XOR gate, this paper presents a method to design reversible logic gates with complex and power efficient. In [13], QCA structures have been presented for new reversible gates using conventional 3-input majority voters as the basic unit. At first, a new 3 × 3 reversible gate (RG-QCA) is proposed and a full adder circuit is designed using this optimal gate. Then, another configuration of RG-QCA gate that called CRG-QCA is reported, this structure is a 4 × 4 reversible gate. Finally, this gate is used for designing a fault tolerant full adder structure. The design of an ALU using different reversible gates in QCA has been executed by many researchers. In Ref [14], A testable reversible ALU based on the reversible multiplexer (RM) have been implemented in QCA. The proposed reversible multiplexer (RM) is composed of three irreversible 2:1multiplexers, and also having 100% fault tolerance ability of QCA technology. In Ref [15] and Ref [16], the structures of reversible ALU are designed by using RUG gate. All circuits in these papers have the same schematic but the QCA layout of these structures is different. In comparison with proposed circuits in [14], these circuits need less constant inputs and generate less garbage outputs. Also, for QCA structure introduced in [16] the occupied area has been significantly reduced, because it has less cells. In Ref [17], designing of an 8-bit reversible ALU with targets to reduce the number of transistors is offered. The suggested ALU is designed by cascading 1-bit ALUs. Furthermore, the COG Gate (Control Output Gate) and the HNG Gate (Haghparast and Navi Gate) has been used as the basic gates.

4. Proposed reversible gate

4.1. Novel reversible gate

In this section, we introduce a new 3×3 Reversible Universal Gate. The block diagram of this gate and its truth table are shown in Fig. 3 and Table 1, respectively. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by $P = A$, $Q = B \oplus C$ and $R = AB + A'C$.

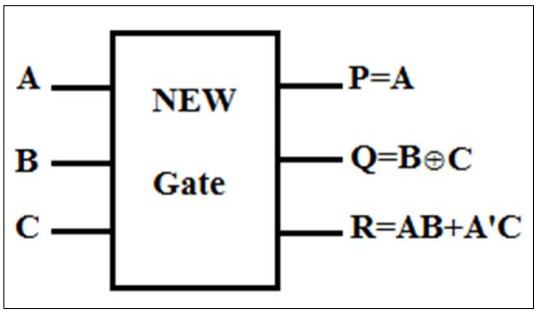


Fig 3: Block diagram of the proposed gate

Table 1 can an adequate reason prove reversibility of the proposed reversible gate because the number of inputs and outputs are equal and a unique output vector can be generated from a unique input vector. As shown in Fig. 4 (a), the proposed gate requires two XOR gates and one majority gate. Fig. 4 (b) demonstrates the graphical symbol of the proposed reversible gate. Furthermore, Output R is obtained as follows:

$$R = M((A \oplus C), B, C) = M(A'.C + A.C', B, C) = A.B + A'.C \quad (3)$$

Table 1: Truth table of the proposed gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1

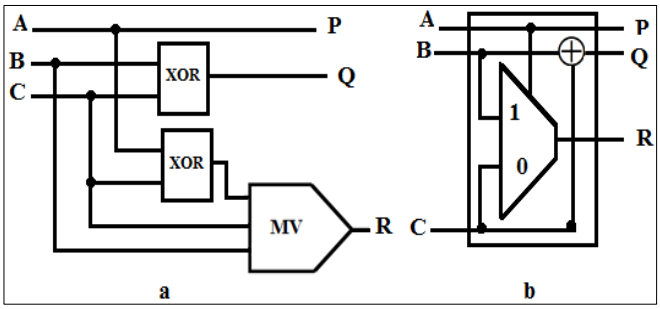


Fig 4: The proposed reversible gate (a) schematic and (b) symbol

4.2. The proposed reversible gate as a universal structure

In general, if a gate can implement all the seven basic Boolean functions (NOT, AND, NAND, OR, NOR, Ex-OR, Ex-NOR) is said to be universal gate. In this state, all Boolean functions can be created by using this gate. Therefore, the proposed gate is a universal because all the basic logic functions can be implemented using the various inputs of this gate. Implementation of the basic logic function using the proposed gate is shown in Table 2.

Table 2: Implementation of the basic boolean functions using the proposed gate

	Logic gate	The inputs required
1.	NOT	(A,0,1)
2.	AND	(A,B,0)
3.	NAND	(A, $\bar{B}$,1)
4.	OR	(A,1,C)
5.	NOR	($\bar{A}$,$\bar{B}$,0)
6.	Ex-OR	(A,B,C)
7.	Ex-NOR	(A, $\bar{B}$,C)

4.3. Realizing standard functions using the proposed reversible gate

In this section, we compare the proposed gate with the previous works, this gate can execute 13 standard functions considered in [18]. According to Fig.5, These thirteen functions can be implemented by using the proposed gate. In Table 3, the average number of required gates to design these standard functions by the proposed gate has been compared with the other gates. As mentioned in Table 3 the average number of gates for the proposed reversible gate is less than Toffoli, Fredkin and RUG gates.

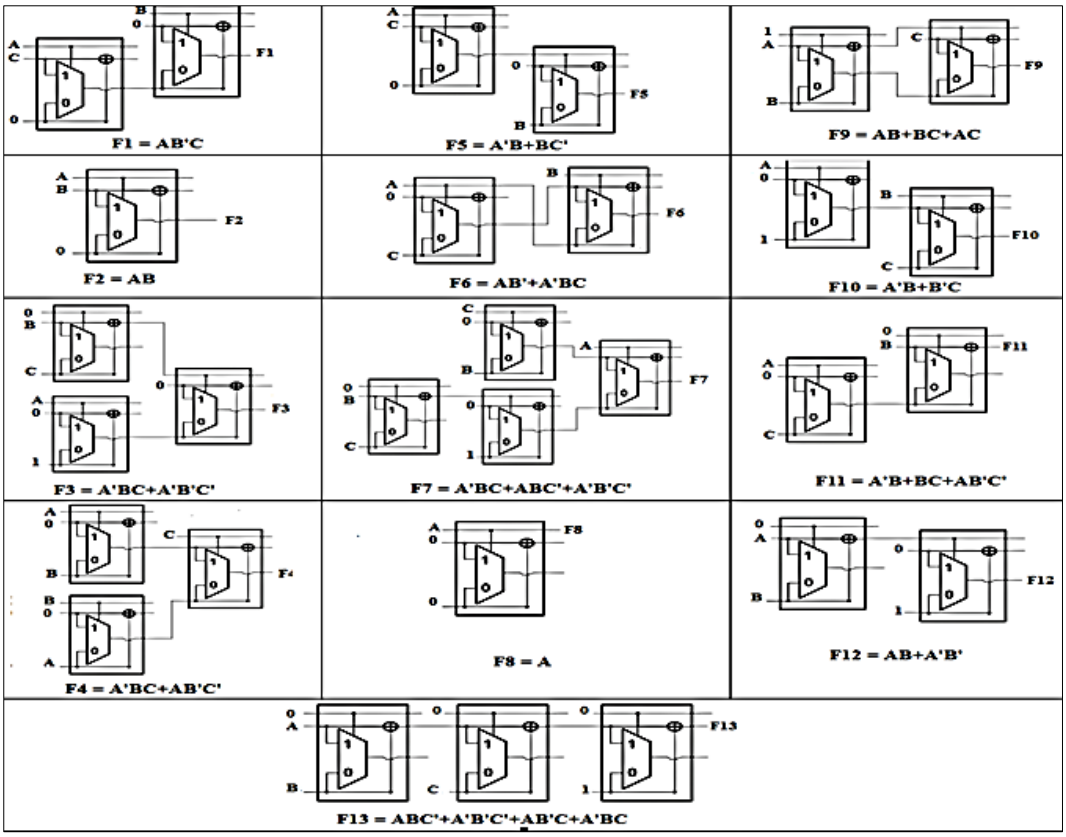


Fig 5: Reversible implementation of the13 standard functions

Table 3: Reversible gate implementation of thirteen standard functions

No.	Standard function	Toffoli gate reported in [19]	Fredkin gate reported in [19]	RUG gate reported in [19]	RM gate reported in [19]	Proposed gate
1	AB'C	2	2	3	2	2
2	AB	1	1	1	1	1
3	A'BC+A'B'C'	3	3	2	2	3
4	A'BC+AB'C'	4	2	3	3	3
5	A'B+BC'	2	2	3	2	2
6	AB'+A'BC	3	2	3	2	2
7	A'BC+ABC'+A'B'C'	5	4	3	3	4
8	A	1	1	1	1	1
9	AB+BC+AC	4	4	1	5	2
10	A'B+B'C	3	1	3	1	2
11	A'B+BC+AB'C'	1	4	3	2	2
12	AB+A'B'	1	2	1	2	2
13	ABC'+A'B'C'+AB'C+A'BC	3	4	3	2	3
Total number of gates		33	31	30	28	29
Average Number of gates		2.53	2.38	2.3	2.15	2.2

4.4. QCA Implementation of the proposed reversible gate

Exclusive-OR (XOR) gate is one of the important gates that it is used in designing digital circuits. As mentioned in the previous section, we need two XOR gates to design a proposed reversible gate, therefore we must use a structure for XOR gate that includes features such as efficiency, high speed and low power. Several structures have been introduced by different authors [20-23]. Hence, we use a new QCA structure for QCA layout which is presented in [24]. This structure is designed in a single layer without any wire crossing and it has only 12 cells.

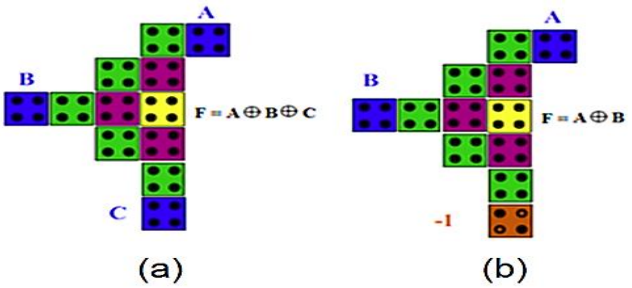


Fig 6: The layout of proposed XOR gate in [24], (a) 3-input XOR, (b) 2-input XOR.

The QCA layout of the proposed reversible gate with coplanar crossover is shown in Fig. 7. For design its structure has been used 148 cells that it requires 1 clock cycle to generate the correct output, and also covered area is 0.17 μm^2. Fig. 8 illustrates the simulation results obtained from QCA Designer tool.

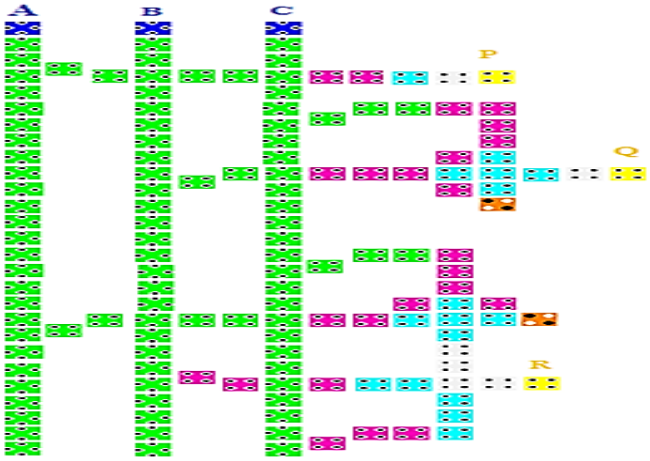


Fig 7: The QCA layout of proposed reversible gate

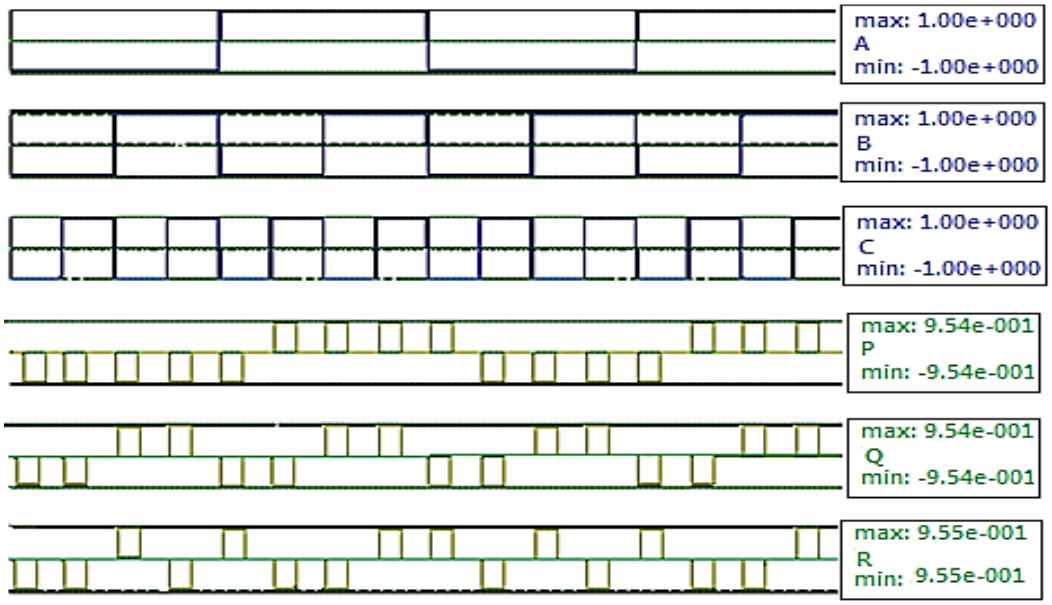


Fig 8: The simulation result of the proposed reversible gate

The reference [25] shows that the average power consumption per cell is almost equal for different QCA adders, it follows that Power ≡ Complexity [25]. The cost of QCA circuits depends on area, delay and power [26], which is obtained as follows:

Cost = *Area* x *Delay* x *Power* (4)

Overall Cost = *Average Gates Number* x *Cost* (5)

In Table 4, the present structure in Fig 7 is compared with RM and RUG gates in terms of the number of cells, area, delay, cost and overall cost. The overall costs of the proposed gate 54% and 57.8% and 54.74% are reduced compared to RM and RUG gates in [14-15], and [16], respectively.

Table 4: Comparison between the proposed gate and RM and RUG gates in QCA technology

Reversible gate	Number of gates*	QCA layout				Cost	Overall Cost
		Cell count	Area (μm^2)	Delay (Clock)	Cross over type		
RM[14]	2.15	224	0.25	1	Coplanar	56	120.4
RUG[15]	2.3	211	0.27	1	Coplanar	56.97	131.03
RUG[16]	2.3	178	0.22	1.25	Coplanar	48.95	122.3
Proposed gate	2.2	148	0.17	1	Coplanar	25.16	55.35

*Average Number of reversible gates for build a 13 standard functions.

4.5. Fault modeling and QCA defects of the proposed reversible gate

The Previous researches show that Defect in QCA manufacturing can occur in chemical synthesis and deposition phase [27]. The possible fault in deposition phase in which QCA cells are missing or additional is more likely to occur [28]. In this paper, we assume the missing cells and the possible fault for the proposed reversible gate. In the following, for investigation the possible defective models of MVs, we consider eight possible input vectors and possible missing cells in the majority gates. Fig.9 represents the cells that are possible to be missed. Table 5 shows the results of defects in the proposed gate. A_i denotes the 3-bit binary pattern whose decimal value is i (e.g. A_0 = 000, A_6 = 110). FP_i denotes the i th applied fault pattern to the under test reversible gate. FT (Fault-Tolerant) shows the percentage of the correct patterns.

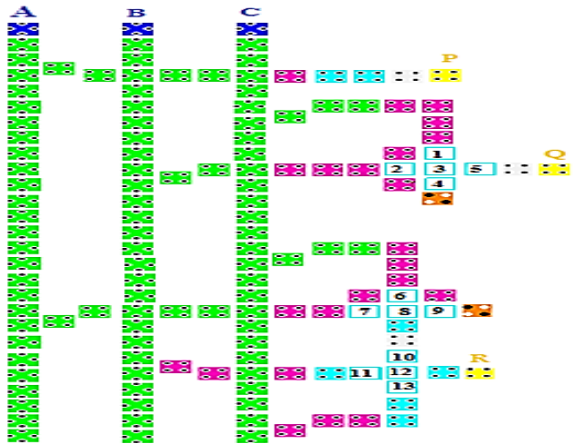


Fig 9: The layout of possibility missing cells of the proposed gate

Table 5: Simulation results of the proposed gate for the defects

Input vector	Fault free vector	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}	R_{13}	% FT
A_0=000	O_0=000	O_0	O_0	010	O_0	O_0	O_0	O_0	O_0	O_0	O_0	O_0	001	O_0	84.6
A_1=001	O_1=011	001	O_1	O_1	O_1	O_1	O_1	010	O_1	O_1	010	O_1	010	010	61.5
A_2=010	O_2=010	O_2	000	O_2	O_2	O_2	O_2	O_2	011	011	011	O_2	011	011	53.8
A_3=011	O_3=001	O_3	O_3	011	011	O_3	O_3	O_3	O_3	O_3	O_3	O_3	000	O_3	76.9
A_4=100	O_4=100	O_4	O_4	110	O_4	O_4	O_4	O_4	O_4	O_4	O_4	O_4	101	O_4	84.6
A_5=101	O_5=110	100	O_5	O_5	O_5	O_5	O_5	O_5	111	O_5	O_5	111	O_5	O_5	76.9
A_6=110	O_6=111	O_6	101	O_6	O_6	O_6	110	O_6	O_6	O_6	O_6	110	O_6	O_6	76.9
A_7=111	O_7=101	O_7	O_7	111	111	O_7	O_7	O_7	O_7	O_7	O_7	O_7	100	O_7	76.9

4.6 AOP Analysis of the proposed reversible gate

In this section, we want to find a temperature range by using the Average Output Polarization (AOP). In this manner, the effective performance range of the proposed gate is determined. The AOP depends on the temperature and is calculated for the specific temperatures as follows.

$$AOP = \frac{\text{Max. Polarizati on - Min. Polarizati on}}{2} \quad (6)$$

We have analyzed the AOP of the proposed gate with the coherence vector simulation engine in QCA Designer software. The default factors are listed as: cell size = 18 nm, relative permittivity = 12.90, clock high = 9.8e-22 J, clock low = 3.8e-23 J, layer separation = 11.5 nm, clock amplitude factor = 2.00 and highest iterations for each sample = 100. The AOP results of the proposed gate in different temperature levels (0-25k) are obtained using equation 6. For example, at temperature T = 3K maximum polarization of output cell P found to be 9.5e-001 and minimum polarization is-9.5e-001, so the AOP for the output cell P is 3.5. The results for different temperatures are illustrated in Fig.10 and we are shown that the strength AOP of the outputs are gradually decreased and when temperature is below 10 K the output terminals P and Q can operate competently. Also, we can see that the strength of AOP of cell R is gradually decreased and when temperature is below 11.5 K, the output terminal R operates efficiently so the proposed reversible gate in the temperature range of 1-10k operates efficiently. In [15] and [16] have been reported when temperature is below 11 K, the output terminals of RUG gate operate efficiently so the RUG gate is robustly up to a larger value of temperature in comparison to the proposed reversible gate.

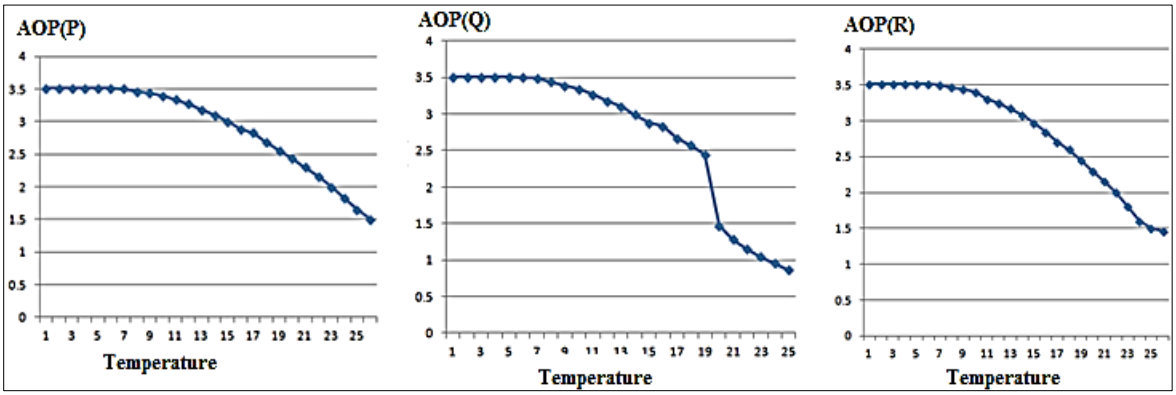


Fig 10: Temperature variation effect on AOP of the proposed gate

5. Proposed Reversible ALU

In today's world, an ALU is the main component of digital circuits and is very important part of the CPU. A RALU is created using reversible logic gates and it consists of the RLU and RAU. The block diagram of the proposed RALU is shown in Fig.11. The SEL line determines which one of these operations can in the output of this circuit.

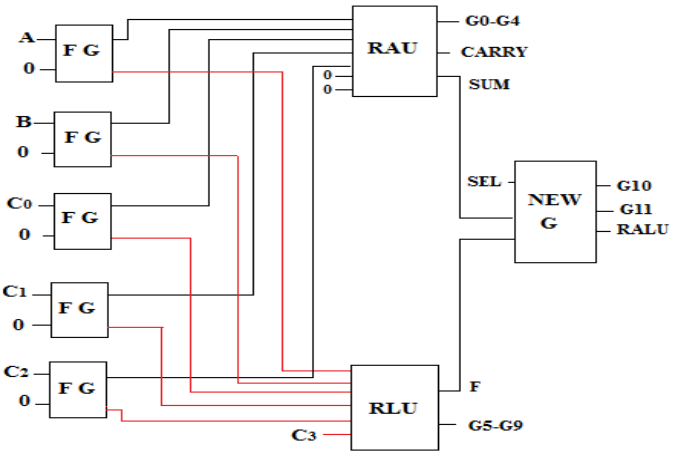


Fig 11: Schematic diagram of the proposed reversible ALU

5.1 The QCA Proposed Architectures

In this section, we are presenting an efficient structure for reversible arithmetic unit (RAU) and reversible logic unit (RLU). These circuits are utilized to design a high performance reversible arithmetic logic unit (RALU). The proposed reversible gate is used as the basic part for the proposed architectures.

According to Fig. 12, the proposed RAU is designed with one Peres gate and three of the proposed gate. The RAU has 7 inputs and 7 outputs which two of its inputs are constant and G_0, G_1, G_2, G_3, G_4 are the garbage outputs. Arithmetic operations mentioned in Table 6 are obtained by using the inputs C_0, C_1 and C_2. Fig.13 shows the QCA layout of proposed circuit. This structure consists of 558 cells, covered area 0.78μm^2 and 3.75 clock cycles.

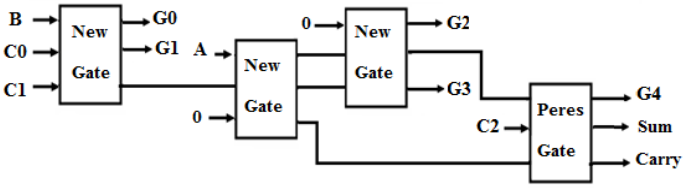


Fig 12: Schematic diagram of the proposed RAU

Table 6: Functionalities of RAU

C_0	C_1	C_2	R	Operation
0	0	0	A	Transfer A
0	0	1	A + 1	Increment A
0	1	0	A + B'	Subtract with borrow
0	1	1	A+ B' +1	Subtraction
1	0	0	A+B	Addition
1	0	1	A+B+1	Add with carry
1	1	0	A+1	Increment A
1	1	1	A-1	Decrement A

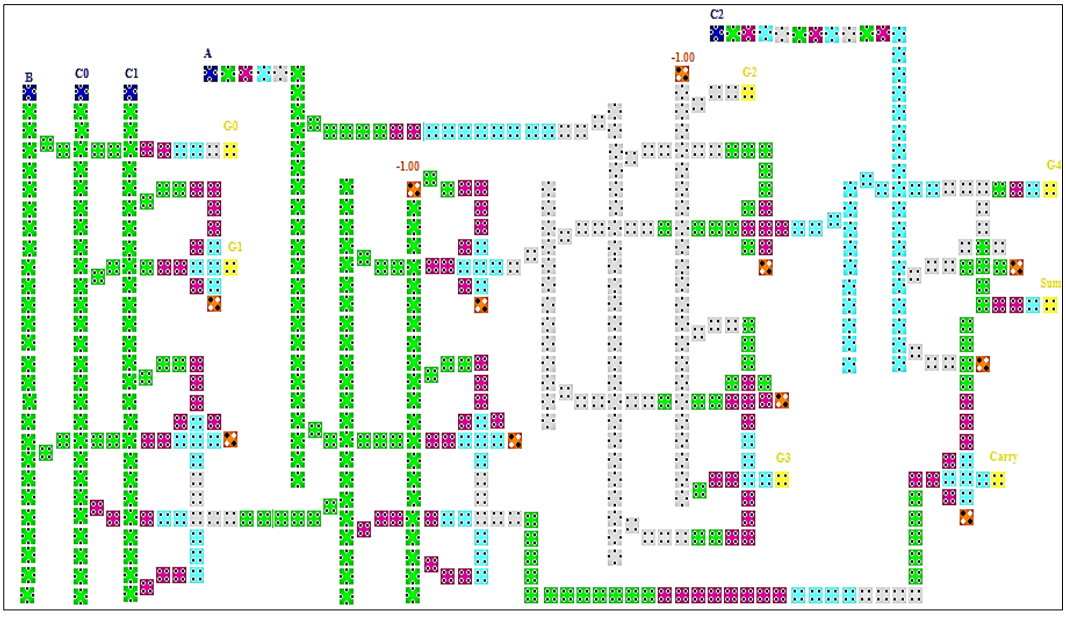


Fig 13: The QCA layout of the proposed RAU

5.1.2 The Proposed Reversible Logic Unit

The proposed unit is able to perform some logical operations like: AND, OR, NOT, NAND and XOR. Furthermore, the introduced design has 6 inputs and 6 outputs, the garbage outputs are shown G_0, G_1, G_2, G_3, G_4. As shown in Fig.14, we used three times of the proposed reversible gate in our design. The logical performance of this RLU is given in Table 7. Also, Boolean equation of the RLU is obtained as follows:

$$F = A' BC_0 + A'B'C_2 + AB'C_3 \quad (7)$$

The QCA layout of RLU is given in Fig. In this structure is using 471 numbers of cells for QCA implementation, which covers an area about 0.61μm^2, its delay is 2.5 clock cycles.

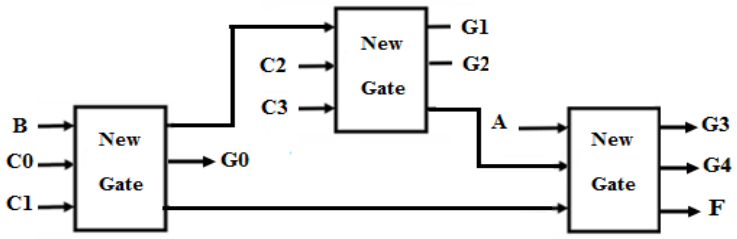


Fig 14: Schematic diagram of the proposed RLU

Table 7: Functionalities of the proposed RLU

C_0	C_1	C_2	C_3	F
0	0	0	0	0
0	0	1	0	AND
0	0	1	1	A = COPY
0	1	0	0	NOR
0	1	0	1	B'= NOT
0	1	1	0	XNOR
1	0	0	1	XOR
1	0	1	0	B = COPY
1	0	1	1	OR
1	1	0	0	A'= NOT
1	1	0	1	NAND
1	1	1	1	1

5.1.3 The proposed reversible arithmetic and logic unit

In this section, according to the block diagram presented in Fig.11, the QCA layout of proposed ALU is shown in Fig.16. This structure is implemented by using 7 new gates and, it has 7 constant inputs and 12 garbage outputs.

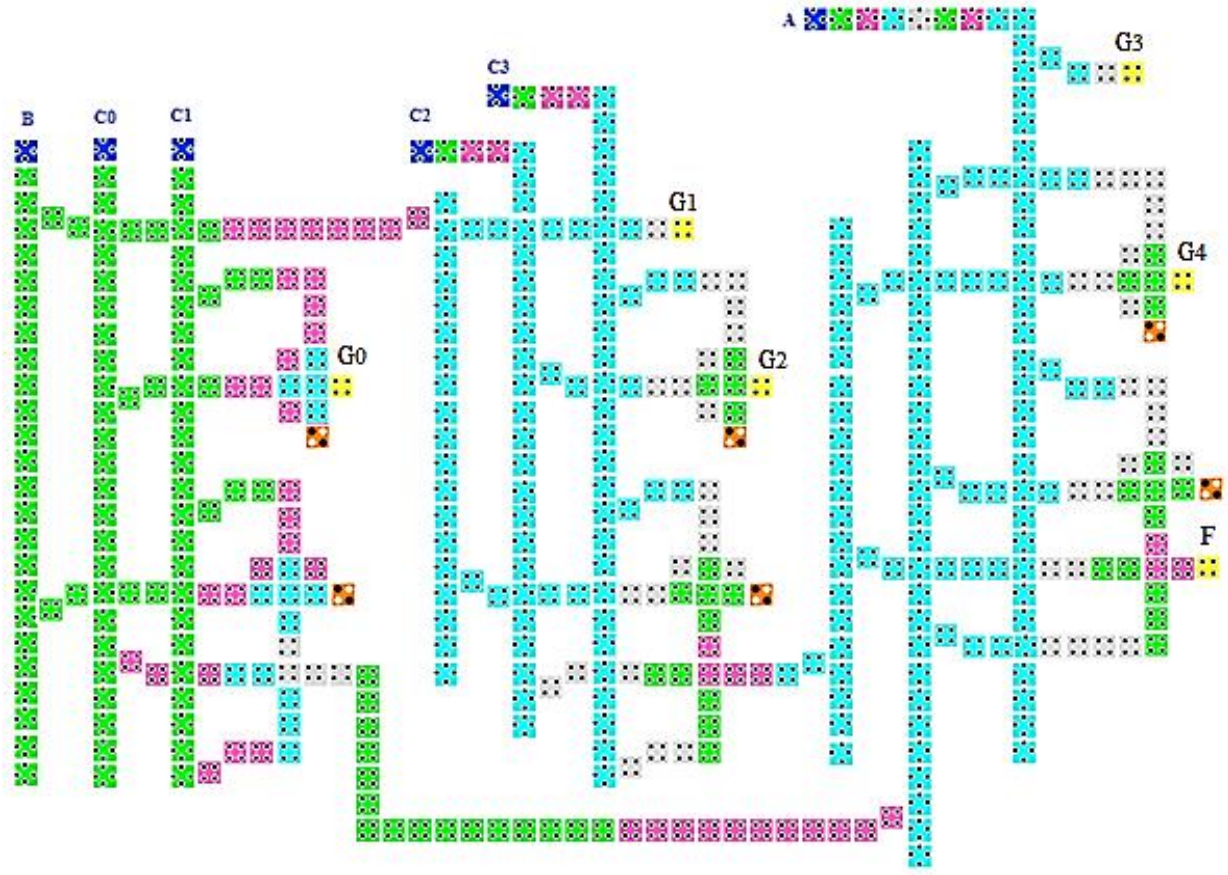


Fig 15: The QCA layout of the proposed RLU

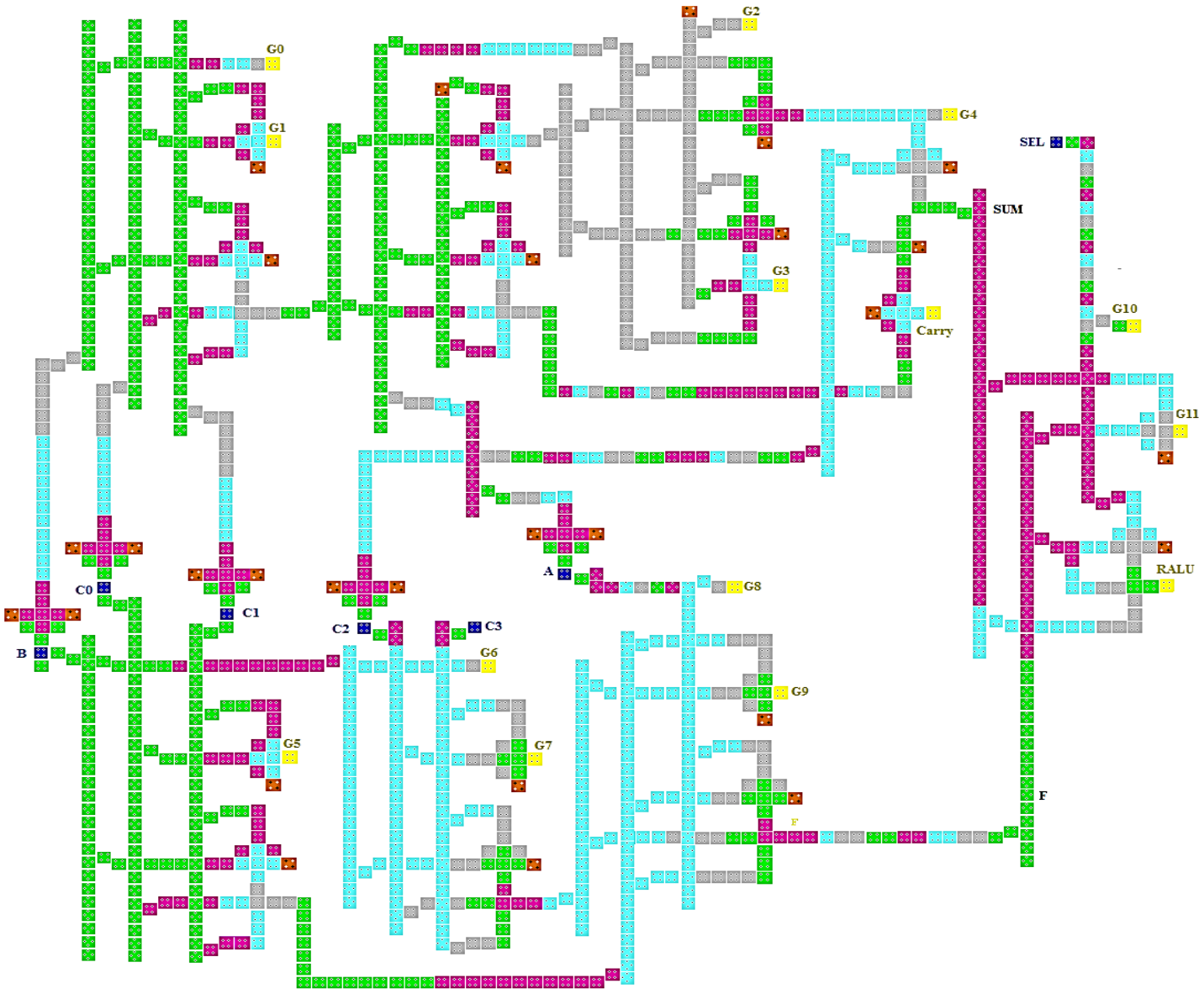


Fig 16: The QCA layout of the proposed reversible ALU

5.2 The simulation results

In this section, we simulate all proposed reversible structures by QCA Designer version 2. 0.3. Some parameters of these simulations such as the dimension of the basic quantum cell and center-to-center space for adjacent cells are default values in QCA Designer.

5.2.1 The proposed reversible arithmetic unit

The simulation result of the proposed reversible structure can be seen in Fig. 21, in our simulation has been used the Bistable simulation engine for evaluating the performance of reversible QCA RLU. In this way, the following parameters are used for the Bistable approximation engine: Number of samples = 6400, Convergence tolerance = 0.001, Radius of effect = 45nm, Relative permittivity = 12.9, Clock high = 9.8e-022, Clock low = 3.8e-023, Clock shift = 0, Clock amplitude factor = 2, Layer Separation = 11.5, Maximum iteration per sample = 100.

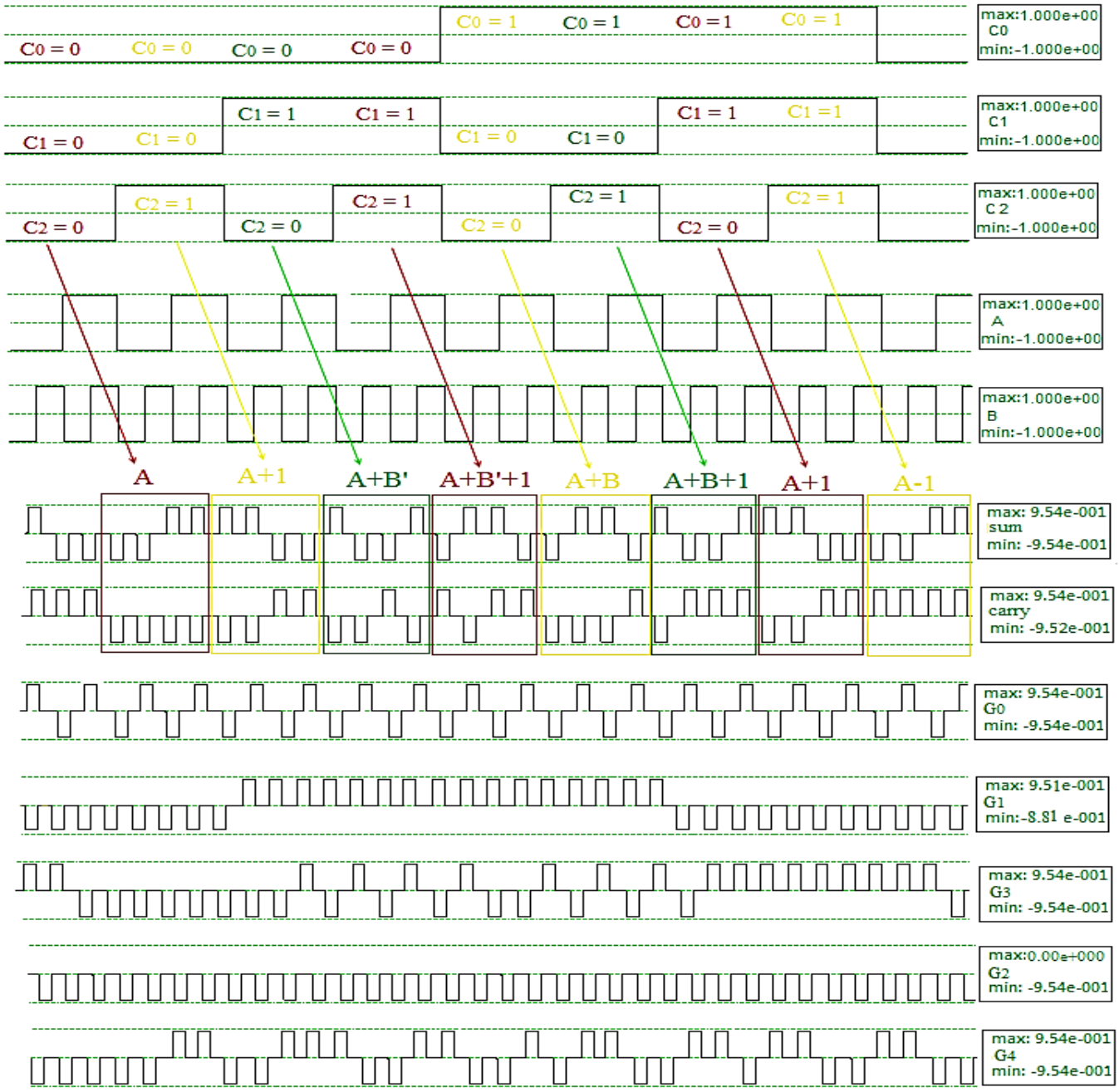


Fig 17: The simulation results of the proposed RAU

5.2.2 The proposed reversible logic unit

The simulation result of the proposed RLU is presented in Fig.16. According to Fig. 18, after 3 clock cycles delay, the Outputs are calculated. The used parameters for simulation are as follows: Number of samples=12800, Convergence tolerance= 0.001, Radius of effect=45nm, Relative permittivity=12.9, Clock high=9.8e-022, Clock low=3.8e-023, Clock shift=0, Clock amplitude factor=2, Layer Separation=11.5, Maximum iteration per sample=100.

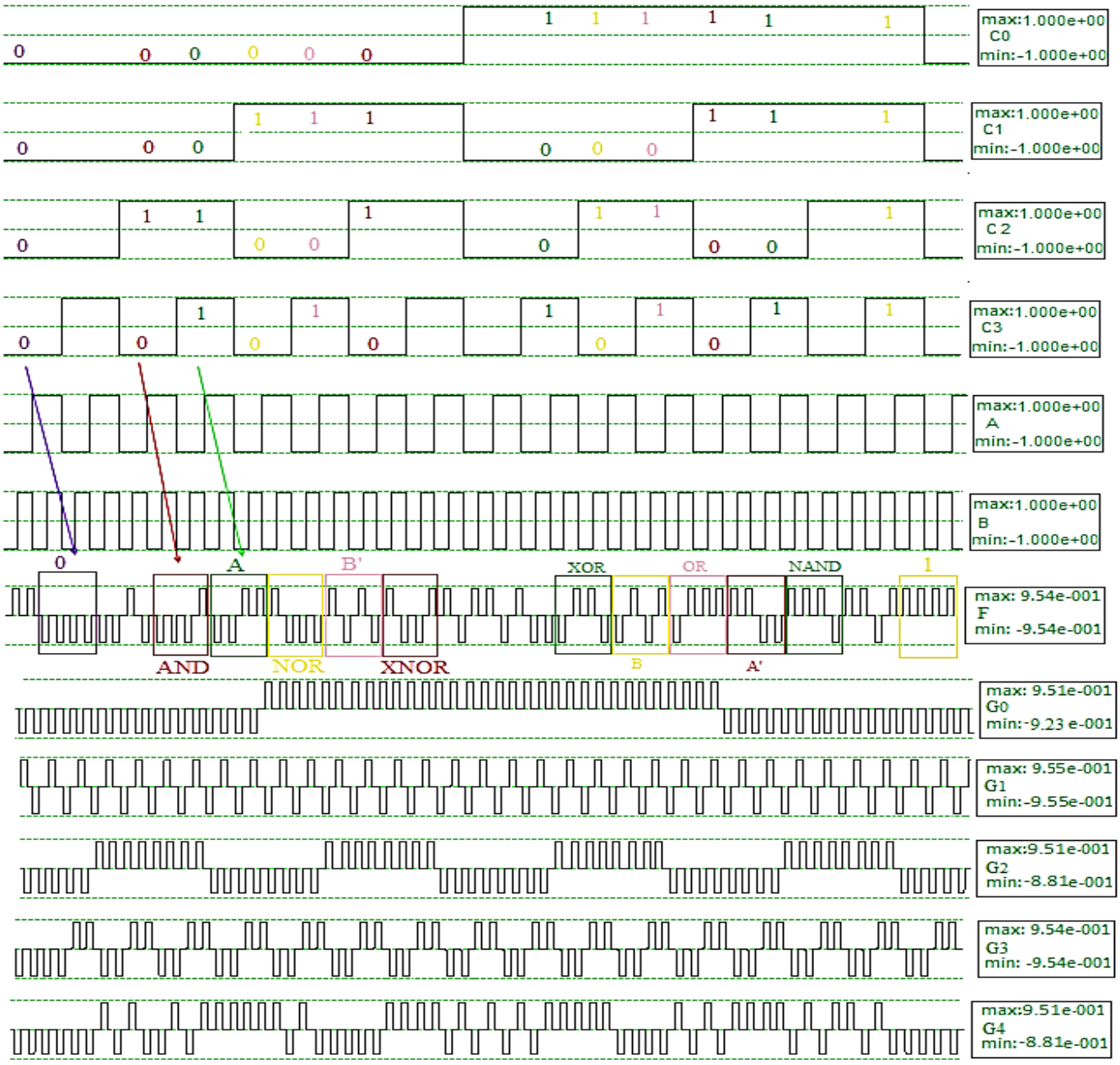


Fig 18: The simulation results of the proposed RLU.

5.2.3 The proposed reversible arithmetic and logic unit

The QCA Designer software based simulation result of the proposed reversible ALU is shown in Fig.19. According to Fig.19, it can be seen that the circuit performs correctly, for this structure by using the Bistable approximation engine the following parameters are used: Number of samples=280000, Convergence tolerance=0.001, Radius of effect=45nm, Relative permittivity=12.9, Clock high=9.8e-022, Clock low=3.8e-023, Clock shift=0, Clock amplitude factor=2, Layer Separation=11.5, Maximum iteration per sample=100.

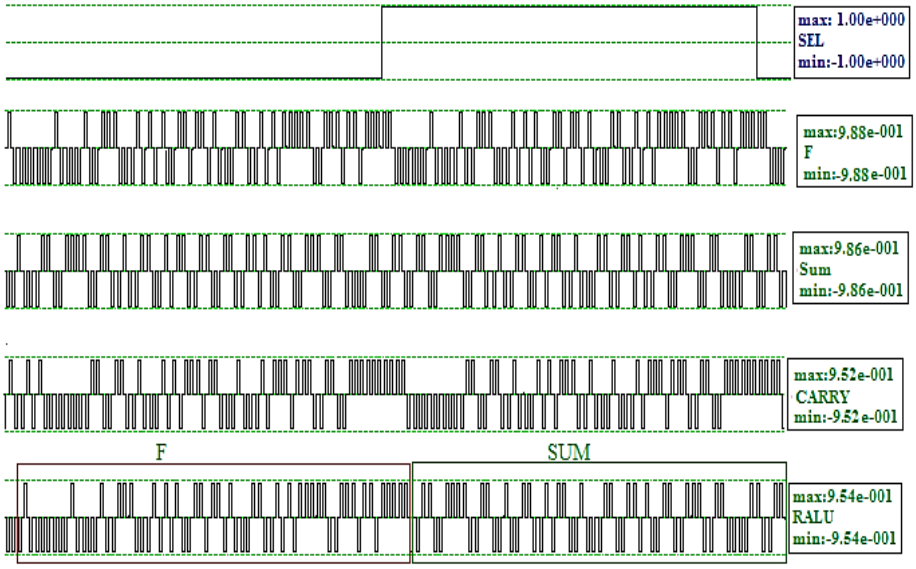


Fig 19: The simulation results of the proposed RALU.

5.3 The performance comparison

In Table 8, a comparison is done between the proposed RAU, RLU and RALU and presented designs in [13, 14, 20] in terms of the majority gate, Constant input, garbage output and delay (clock zone). The proposed RAU has 33.3%, an improvement in majority voters. The proposed RLU has 62.5%, 16.6% improvement in majority voters and delay respectively, and the reversible ALU has 62.5% improvement in majority voters. In Table 3 it was shown that the proposed reversible gate has the lowest cell count and area in comparison with the previous works so we can say that all the proposed design base on this gate have the lowest cell count and area.

Table 8: Comparison between the proposed designs and previous works

Various designs	Type of structure	MV	Constant input	Garbage output	Clock
	RAU	40	3	6	5
Ref [14]	RLU	40	1	7	3
	RALU	105	9	15	-
	RAU	18	0	3	4
Ref [15]	RLU	24	1	6	3
	PALU	68	6	11	8
	RAU	18	0	3	3.25
Ref [16]	RLU	24	1	6	3.25
	RALU	64	6	11	5.25
	RAU	12	2	5	3.75
Proposed designs	RLU	9	0	5	2.5
	RALU	24	7	12	5.25

6. Conclusion

In this paper, an improved design of fault-tolerant one bit reversible ALU in Quantum-dot Cellular Automata is presented which use coplanar crossover. For design an efficient one bit reversible ALU, a new 3*3 reversible gate has been offered which contains 148 cells and its occupied area is 0.17 μm^2. In addition, for evaluating its performance, it has been studied by implementation of thirteen standard functions. According to simulation results, this gate has the lowest cost and overall cost with compared to the previous works. Also, the reversible ALU structure is made of RAU and RLU blocks. These designs achieved a significant improvement in the number of majority gates, cell counts and covered area. For further research, we will design more reversible digital circuits using the proposed 3*3 reversible gate and will expand this work in 2-bit, 4-bit and 8-bit reversible ALU.

7. References

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